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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,890	02/02/2004	James M. Derderian	2269-4817.3US (01-0103.03	1094

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,890	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/2/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. This application appears to be a Continuation of Application No. 10/446,382, filed 5/27/03.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1-14, 16-25** and **31-33** are rejected under 35 U.S.C. 102(b) as being anticipated by Ball (5,291,061).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims **1-14, 16-25** and **31-33**, Ball teaches (see specifically figures 1-2, Col. 3 and 4) a method for forming a multi-chip module, comprising: providing a substrate (14) including a plurality of contact areas (36); providing a first semiconductor device (20) on the substrate; establishing electrical communication between the substrate and the first semiconductor device (20), wherein establishing electrical communication

comprises placing discrete conductive elements (e.g., bonding wire 30N) extending partially over the active surface of the first semiconductor device (20), applying substantially a predetermined volume of adhesive material (e.g., thermoplastic adhesive 22) at least to the active surface of the first semiconductor device (20) to space the active surface apart from a back side of a second semiconductor device (18), which is placed on the first semiconductor device (20), substantially curing the adhesive material; encapsulating at least portions of the first and second semiconductor devices, the discrete conductive elements and the substrate.

4. Claims **1-14, 16-25** and **31-33** are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al (5,323,060).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims **1-14, 16-25** and **31-33**, Fogal et al teach (see specifically figures 1-6, Col. 2-4) a method forming an assembly including semiconductor devices in stacked arrangement, comprising: providing a substrate (12) including a plurality of contact areas (e.g., where bonding wires 44-50-56 electrical connected); providing a first semiconductor device (18) on the substrate; placing bonding wires (44-50-56) between bond pads (26) on an active surface of the first semiconductor device (18) and corresponding contact area of the substrate (12), wherein the bonding wires (44-50-56) comprises discrete conductive elements (e.g., the bonding wires' portions connected to the bond pad 26 of the semiconductor device) extending partially over the active surface of the first semiconductor device (18), applying substantially a predetermined volume of

adhesive material (38) at least to the active surface of the first semiconductor device to space the active surface apart from a back side of a second semiconductor device (28), which is placed on the first semiconductor device, wherein the adhesive material draws the second device toward the first device until the first device and the second device are spaced substantially a set distance apart (48) from one another; substantially curing the adhesive material.

5. Claims **1-25** and **31-33** are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (6,333,562 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims **1-25** and **31-33**, Lin teaches (see specifically figures 3-10, Col. 4-6) a method forming an assembly including semiconductor devices in stacked arrangement, comprising the steps: providing a substrate (e.g., a circuit board) (330) including a plurality of contact areas (330a); providing a first semiconductor device (310), which has a plurality of bonding pads (310a) formed on the active surface thereof, on the substrate (330) (Fig. 5); placing discrete conductive elements (e.g., bonding wires) (360) between bond pads 350a of the first semiconductor device (310) and corresponding contact areas (330a) of the substrate (330) to electrically connect the bond pads to the corresponding contact areas, wherein the discrete conductive elements (350b) extend partially over an active surface of the first semiconductor device (310) (Fig. 6). Lin further discloses the process steps: applying a volume of adhesive material (340) to the active surface of the first semiconductor device (310) before positioning the back side of

a second semiconductor device (320) over the adhesive material (340) on the first semiconductor device (310). Since the second semiconductor device (320) is placed into the adhesive material (340) until contacting the protruding portions (350b) formed on the active surface of the first semiconductor device (Col. 5, lines 40-53), the distance between the active surface of the first semiconductor device (310) and the back side of the second semiconductor device (320) is decreased from substantially a set distance to substantially a predetermined distance and. Although Lin does not explicitly teach the volume of adhesive material being "*a substantial predetermined volume of adhesive*" to space the first device apart from the second device by *substantially a predetermined distance*, as claimed, this feature is taken to be inherent in the Lin's process, since "*forming an adhesive layer with a stable bond line thickness*" and "*controlling the space apart from the first semiconductor device (301) to the second semiconductor device (320) by the protruding portions (350b) formed on the active surface of the first semiconductor device*" are disclosed and it is apparent that "*a substantial predetermined volume of adhesive*" must be set to space the first device apart from the second device by "*substantially a predetermined distance*" to construct the semiconductor device in stacked arrangement, as shown in Lin's Figs. 3-4 (Col. 5, lines 40-53). Lin also discloses the steps of substantially curing the adhesive material (Col. 5, lines 54-62) and encapsulating at least portions of the first and second semiconductor devices, the discrete conductive elements (360-370) and the circuit board substrate (330) (see Col. 4, lines 39+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al (5,323,060) in view of Fujisawa et al (5,801,439).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 26-30, Fogal et al method discloses all the limitations of the claimed invention as detailed above except for the adhesive being introduced between the first device and the second device.

Fujisawa et al while related to a similar method of forming semiconductor device in stacked arrangement teach, among the other, a step of inserting an adhesive (101) between two adjacent semiconductor devices (81c-81b-81a) (after mounting the upper device on the lower device) to support the upper side semiconductor device against the lower side semiconductor device (see Fig. 18, Col. 20, lines 59+, Col. 21, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fogal et al by inserting the adhesive material between two stacked device packages in order to support the upper side semiconductor device against the lower side semiconductor device, as taught by Fujisawa et al, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

8. Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (6,333,562 of record) in view of Fujisawa et al (5,801,439).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 26-30, Lin discloses all the method steps of the claimed invention as detailed above except for the encapsulant being introduced between the first semiconductor device and the second semiconductor device.

Fujisawa et al while related to a similar method of forming semiconductor device in stacked arrangement teach, among the other, a step of inserting an adhesive (101) between two adjacent semiconductor devices (81c-81b-81a) (after mounting the upper device on the lower device) to support the upper side semiconductor device against the lower side semiconductor device (see Fig. 18, Col. 20, lines 59+, Col. 21, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lin by inserting the adhesive material between two stacked device packages in order to support the upper side semiconductor device against the lower side semiconductor device, as taught by Fujisawa et al, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2827
June 28, 2004